tant structure.

[0023] Fig. 4A shows alternate processing steps to those of Figs. 3B–D whereby any excess release layer used to form the present vertical interface and the patterned blockout resist layer are either sequentially or simultaneously removed to form the structure of Fig. 3E.

[0024] Fig. 4B illustrates that the vertical interface of Fig. 3F may be formed as a voided release layer channel.

[0025] Fig. 4C illustrates that the vertical interface of Fig. 3F is formed directly adjacent the crack stop to either deflect or absorb any generated cracks during semiconductor processing.

[0026] Figs. 5A–C illustrates the steps of forming the present vertical interface in an ultra low-k dielectric as altered release layer trenches adjacent to a crack stop of the resultant structure, whereby Fig. 5B illustrates that the release layer has been altered by forming a void that weakens adhesion of the present release trench to the crack stop, while Fig. 5C illustrates that the release layer has been altered by changing the dielectric mechanical properties of the release layer to increase its crack resistance adjacent the crack stop, i.e., increase its toughness.

DETAILED DESCRIPTION

invention, the vertical interface may be either altered low-k dielectric layer, or a release material having either low adhesion or sufficient toughness properties as discussed in detail below.

BRIEF DESCRIPTION OF DRAWINGS

[0019] The features of the invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The figures are for illustration purposes only and are not drawn to scale. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows taken in conjunction with the accompanying drawings in which:

[0020] Figs. 1A-G show, in sequence, the steps of forming the vertical interface of the invention as a plurality of individual spacer structures throughout the chip.

[0021] Figs. 2A-F show, in sequence, the steps of forming the present vertical interface in a non-ultra low-k dielectric as release layer trenches adjacent to a crack stop of the resultant structure.

[0022] Figs. 3A-F show, in sequence, the steps of forming the present vertical interface in an ultra low-k dielectric as release layer trenches adjacent to a crack stop of the resul-